Digital Interface IP-II Module

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This note describes a digital interface IndustryPack™† module. Digital Interface Module is an IP module that is used for operation of the Linac-style local station software on the Motorola MVME-162 computer card. It is used as part of the Fermilab Internet Rack Monitor. The main component of the module is an Actel-1240 field programmable gate array. The 1240 gate array is a user programmable chip that can be configured and programmed locally in the Actel development system. Features of the module and the associated FPGA are discussed.

Physically, the IndustryPack Module is a 1.8" by 3.9" circuit board that contains two high density 50-pin "D" female connectors as defined by the GreenSpring IndustryPack specification. This specification is a public domain definition of a small mezzanine board for use in microprocessor-based systems. Four IP module slots are available on the MVME-162 single board computer. Figure 1 is a diagram of the IP digital interface module showing the parts placement including the two 50-pin connectors, one logic interface and one for user I/O signals. Figure 2 is a block diagram of the module. The logic interface includes:

D0-D15	16 bit data
IOSEL/	I/O Addr space select
INTSEL/	Interrupt Select
INTREQ0,1	Interrupt request
MEMSEL/	Memory select
ACK/	Acknowledge
R-W/	Read-Write control
Addr 1..6	I/O space Address lines
Reset/	Clears all registers, inhibits triggers (low active)

This module has two main functions: 1) it provides a place to put circuitry for miscellaneous features needed to make a data acquisition station, and 2) it interfaces the 162 cpu card to an external 8-byte digital I/O board that is part of the Internet Rack Monitor. The Actel chip, called IPDIG6, contains the following circuitry:

- IP logic interface
- 2 Interrupt vector registers
- Control/Status register
- Tevatron-style event clock decoder
- Trigger event register
- 16-bit delay counter
- Divide by 10 clock prescaler
- Byte of Lights Register
- Byte of Switches input
- Interface to offbd digital I/O board
- 64 Byte FIFO for detected clock events

Registers in the Actel part are mapped into the Industry-Pack I/O space. Figure 3 shows the Actel pinout and Figure 4 shows the address map of the module and the individual bits of the control and status register.

The first 32 bytes of IP I/O space are allocated to offboard digital I/O addressed at Base+$00..$1F. The user I/O connector shown in Figure 5 contains a 16-bit data bus and the control signals necessary to store and read back data from offboard registers. As a part of the Internet Rack Monitor development, an external 8-byte digital I/O board will be driven by this IP module. Data direction control for the 8 bytes of digital I/O is controlled by an 8-bit DIP switch. Settings for this switch are read back at address $09. The two most significant bits of address $08 are used to operate small relays that can be used to include the rack monitor in system interlock chains. The external I/O board has two more bytes of LEDs that are used to indicate and time the execution of various tasks in the software. These LED registers are located at $0A and $0B.

Tevatron clock is received by a discriminator that has a self tracking reference input circuit. This design eliminates the need to adjust the input discriminator level for various amplitude input signals. A second discriminator clamps the output of the first discriminator in the absence of an input signal. The cpu may be interrupted by the IP *IntReq0* signal caused by the output of a 16 bit delay timer triggered by any selected clock event or the 15 Hz Booster reset. The normal operation is to interrupt the processor with a pulse delayed from 15 Hz.

In the absence of a Tevatron clock, the IP 8 MHz clock can be selected, CR bit 5, for use as the timbase for the delay timer. In this case an external trigger is needed to start the delay timer. This mode is selected by setting CR bits 4=1 and 3=1 .

The 8-bit value of each clock event is recorded, in a separate 64-byte FIFO memory chip, as soon as the event is decoded. For each event, the *Data Valid* signal from the decoder is used as the FIFO *ShiftIn* pulse. The *Output Ready* signal from the FIFO causes an interrupt to the host processor via the IP's *IntReq1* signal. For some applications, the high rep rate clock events, 15 Hz, 1440 Hz, 720 Hz,

and 60 Hz, are not needed. Storing these high rep rate clock events, $0F, $0E, $07, and $06, can be individually enabled by setting bits 14, 13, 12, and 11, equal to "1", respectively. The FIFO is used on this module, because Tevatron clock events can come at intervals as short as 1.2µs, shorter than the execution time of the interrupt service routine that processes the clock event. Using data collected in the FIFO, the cpu can determine which clock events have occurred. The FIFO output appears as the odd (lsb) byte of a word read at address Base + $22. The even byte (msb) contains the 'output ready', 'input ready', 'half full', and 'almost full/empty' signals as bits 15, 14, 13, and 12 of the FIFO data word, respectively. A write operation to address Base+$21 causes a *Reset* to the FIFO memory chip, clearing all stored data and resetting the *Output Ready* signal.

The timer control register shown in Figure 4, has several unused bits because it is the same design that is used in the predet FPGA and some of the bits do not apply in this case.

The byte of LEDs register and the byte of switches inputs are implemented on the 1240 chip itself to eliminate the need for any external I/O board. "Switch" settings can be wire wrapped on the I/O connector and LEDs are not required. This arrangement would be used when the '162 is mounted in a VMEbus crate rather than being packaged as an Internet Rack Monitor.

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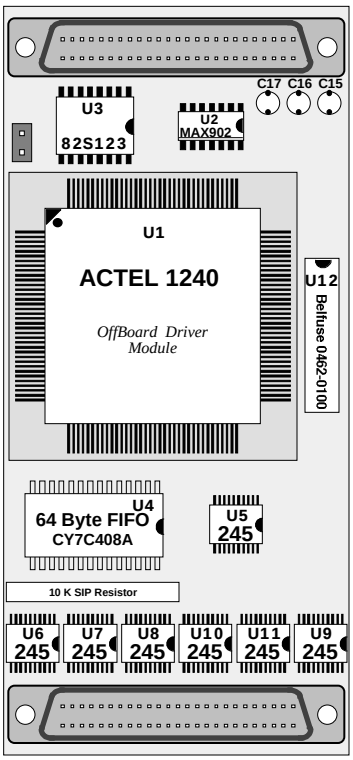

Figure 1. Off Board Interface IP-II Module

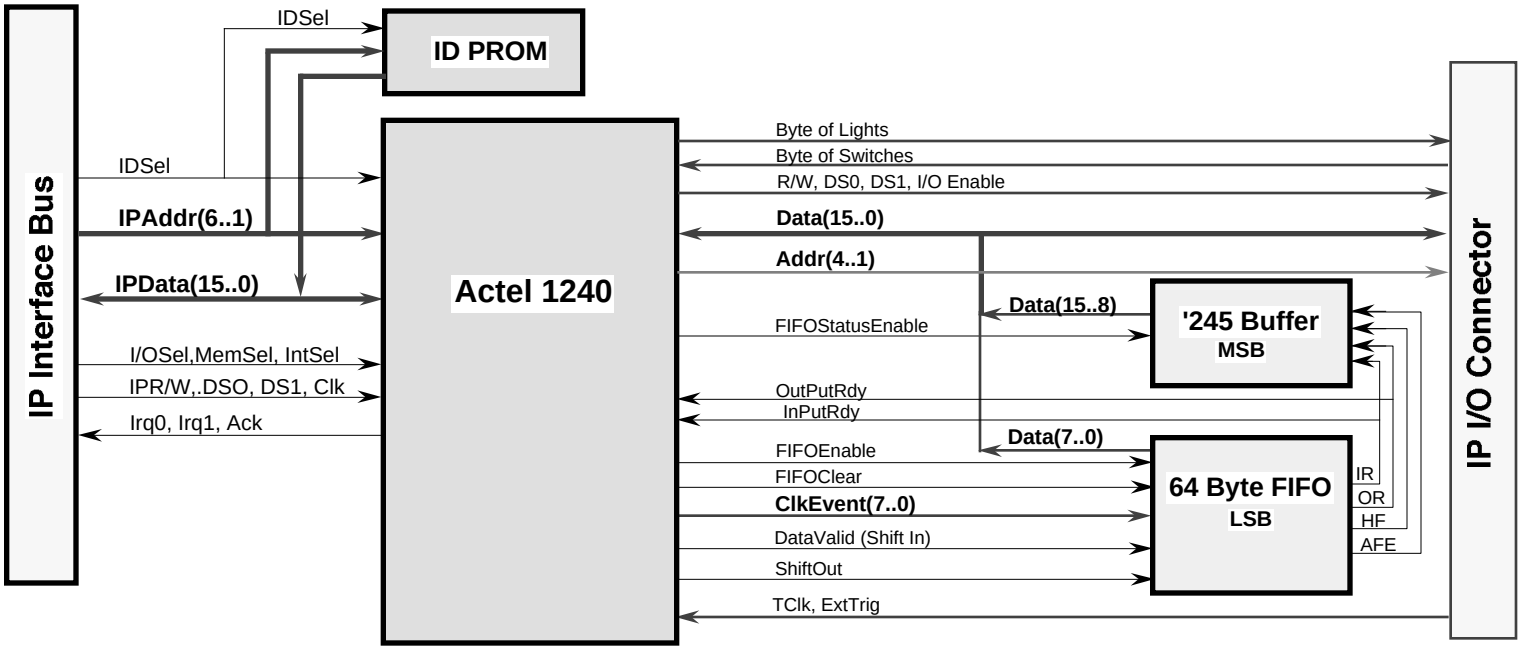

Figure 2. Block Diagram of the Digital I/O Interface IndustryPack

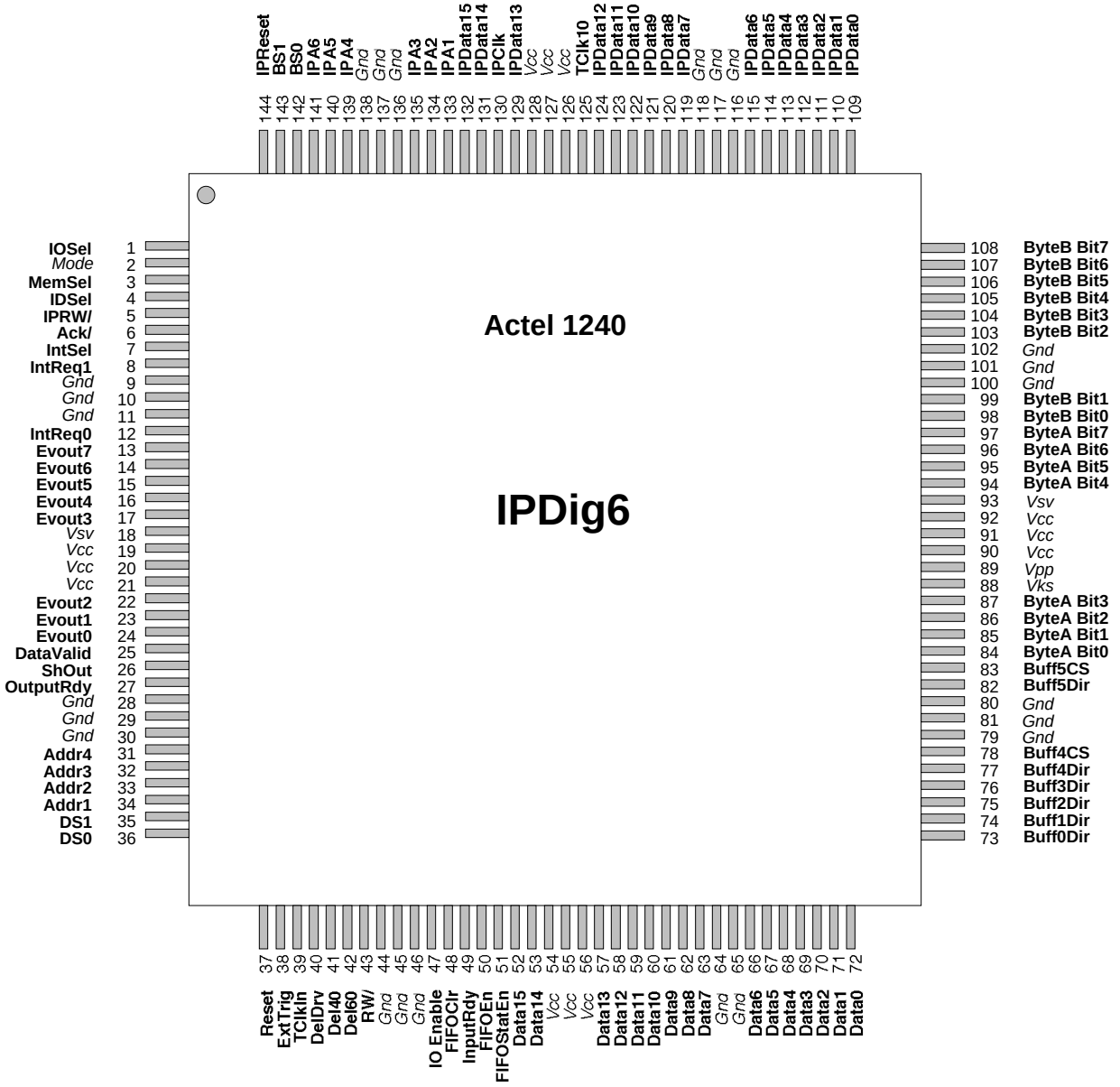

Figure 3. Offboard Interface Actel 1240 Pinout

Address				
Base + $00	Byte0 • Byte1	Byte2 • Byte3	Byte4 • Byte5	Byte6 • Byte7
Base + $08	Relays • DDir	Tsk LEDS0 • Tsk LEDS1	–	–
Base + $10	–	–	–	–
Base + $18	–	–	–	–
Base + $20	LEDS • Switches	FIFO Status•FIFO Data	-	µP Start Delay
Base + $28	– • Trig Event	Int Vect1 • Int Vect0	-	Int1 Ctrl • Tmr Ctrl
Base + $30	–	–	–	–
Base + $38	–	–	–	–

Figure 4a. Memory Map for IPDig6 FPGA

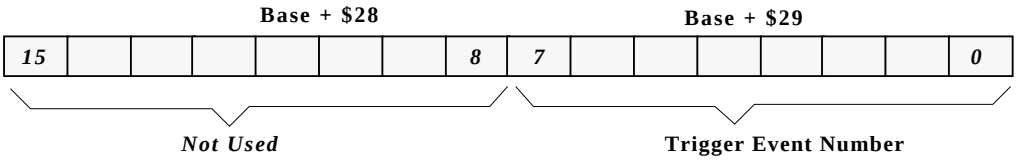

Figure 4b. IPDig6 Event Register

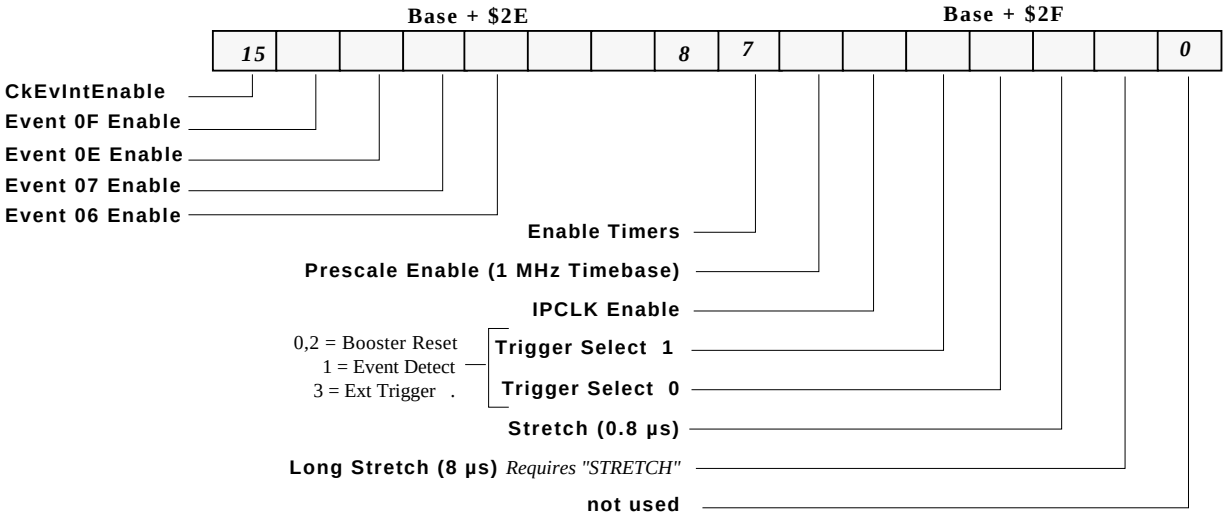

Figure 4c. IPDig6 Control Register

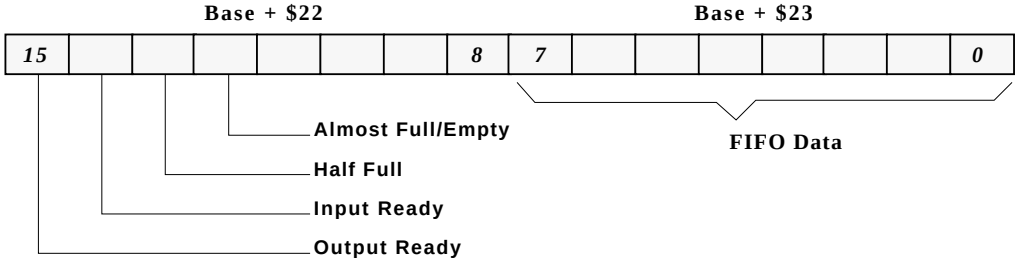

Figure 4d. IPDig6 FIFO Register

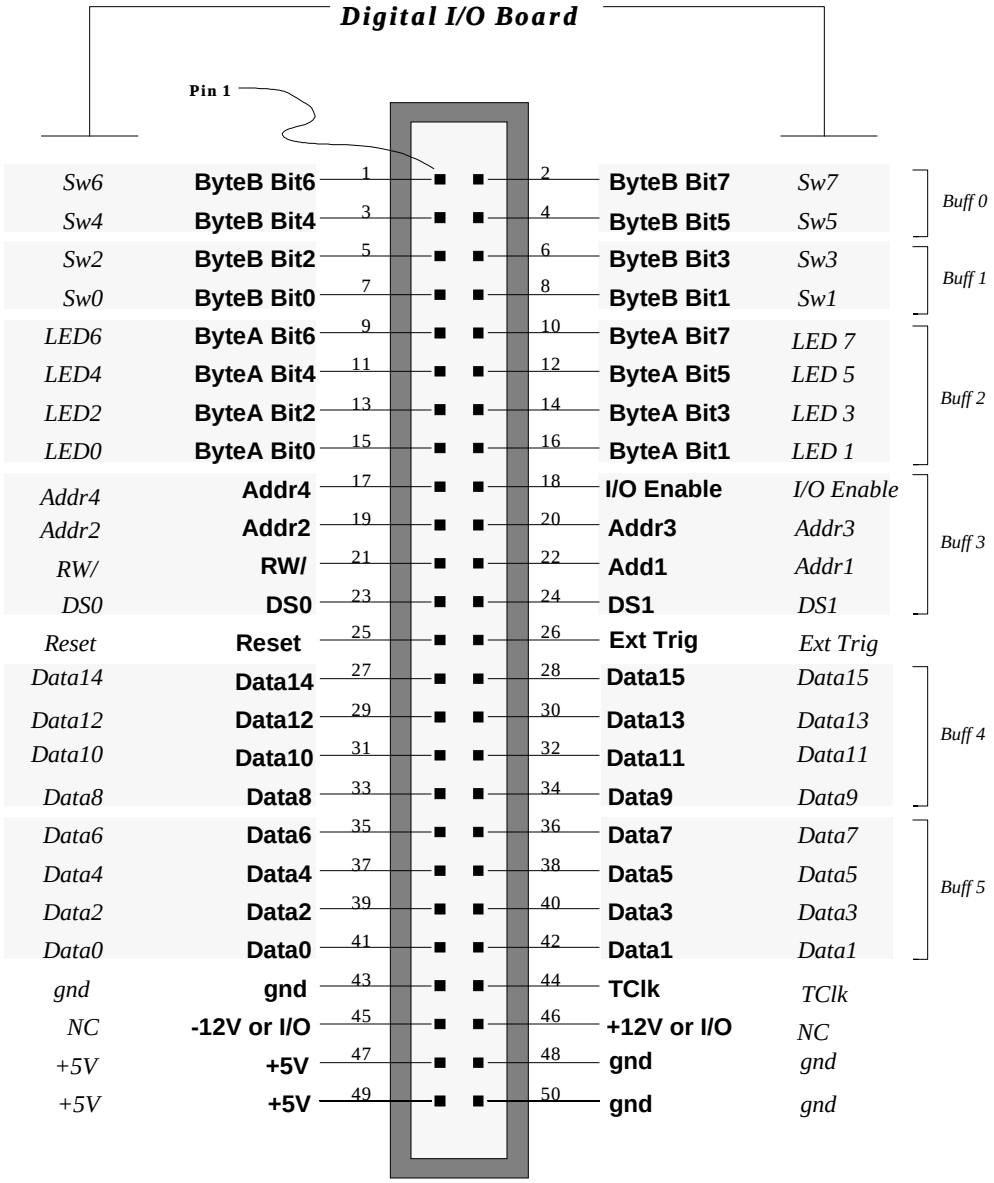

Figure 5. I/O Interface Driver Connector Pinout